Proceedings of the Fifth IASTED International Conference
CIRCUITS, SIGNALS, AND SYSTEMS
July 2–4, 2007, Banff, Alberta, Canada
ISBN Hardcopy: 978-0-88986-669-0 / CD: 978-0-88986-670-6

MODULO-*N* BASED DIGITAL FREQUENCY SYNTHESIZER WITH ENHANCED INPUT FREQUENCIES

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ABSTRACT
With a modulo-*N* accumulator and a set of reference waveforms, a new architecture of high-performance digital frequency synthesizer is devised. The reference waveforms with the same frequency but different phases are passed through a multiplexer to obtain the maximal frequency with an incrementer. A Gray encoder is designed to eliminate the glitch problem. The performance of the synthesizer is illustrated via timing simulations with the TSMC 0.35μm cell-based process.

KEY WORDS
Modulo-*N*, Accumulator, Digital Frequency Synthesizer, Flying Adder

1. Introduction

Frequency synthesizers are used in various applications, such as the signal synchronization, the mixer of communication systems, etc. [1]. There are different ways to realize the frequency synthesizer [1]. In [2] the ideal of modulo-*N* arithmetic was used for digital frequency synthesizer. In [3]-[5], an architecture of frequency and phase synthesizers was designed, which used multiple reference waveforms with different phases from the taps of a ring oscillator. The architecture of [3] can generate a desired frequency in a few cycles with the relative phase offset of reference waveforms, which is well-known as the flying-adder architecture. However, there are some problems associated with the frequency synthesizer devised in [3], such as the noise from long oscillator stages for a higher frequency output, and the glitch problem of the input multiplexer. A two-path structure has been proposed to solve the glitch problem in [3], which results in a larger chip area and higher power consumption. An improved architecture was developed in [5] and [6] to solve some problems of the frequency synthesizer proposed in [3].

In this paper, a new architecture of high-performance digital frequency synthesizers is designed and analyzed (see Fig. 1). The modulo-*N* accumulator and a set of reference waveforms are combined in series, where the reference waveforms with the same frequency but different phases can be generated by a ring oscillator [3] or a series of delay gates. The relative phase offset of the reference waveforms can generate signals with higher frequencies. The reference waveforms are first sent to an *M*-to-1 multiplexer that is controlled by the output of an incrementer to yield the maximal frequency. Then, the multiplexer output with the maximal frequency is sent to the modulo-*N* accumulator which is used to generate the desired frequency with a frequency control word. To avoid the glitch problem, a Gray-code encoder is designed for the selection of the multiplexer input.

As a consequence, the glitch problem is eliminated with smaller chip areas and less power consumption as compared to the two-path flying-adder synthesizer [3]. In addition, by using the modulo-*N* accumulator, the resolution of the synthesized frequencies can be enhanced without increasing noise.

The paper is organized in the following way. In Section 2, the architecture of the modulo-*N* based digital frequency synthesizer is presented. In Section 3, the inherent phase jitter is analyzed, and the maximum phase jitter as a function of the desired frequency is derived. In Section 4, the timing simulation results with the TSMC 0.35μm cell-based process are illustrated for different values of the frequency control words, the theoretical period and the period from simulations are compared, and the numerical results of the phase jitter are given. Conclusions are drawn in Section 5.

2. Architecture

The system architecture of frequency synthesizers is illustrated in Fig. 1 where a 32-to-1 multiplexer is used.

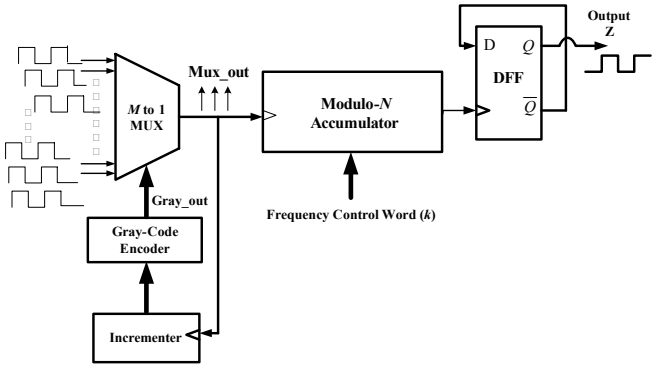

Figure 1: The new architecture of frequency synthesizer based on the modulo-N arithmetic with reference waveforms.

In Fig. 1, the incrementer is an accumulator that adds the unit value to itself every cycle. The M reference waveforms with the same frequency but different phases are input into the multiplexer, and the output of the Gray-code encoder (Gray_out) selects the reference waveform that is most adjacent to the previous selection, and thus results in an output (Mux_out) with the maximal possible frequency that can be generated by the flying-adder structure [3]. When a ring oscillator is used to generate the M reference waveforms as in [3], the smallest phase offset or the maximal frequency of the waveform set is adjustable. The D-type flip-flop (DFF) in Fig. 1 makes the output the desired waveform.

Let the smallest phase offset of the reference waveforms is Δ. Thus, based on the selection of incrementer with Gray_out, the frequency of Mux_out is $1/\Delta$. The practical maximum output frequency will be limited by the critical path of the incrementer. For example, if the processing time of the incrementer is t_{incr}, then the frequency of Mux_out is constrained by

$$f_{mux\_out} \le \frac{1}{t_{incr}}. \quad (1)$$

The system circuit of the modulo-N accumulator is given in Fig. 2, where the accumulator mainly consists of an R-bit adder and an R-stage register, and k is the frequency control word with the range $0 < k \le N$. Once the frequency control word k is changed for generating a different output frequency, the previous frequency control word should be erased and the new value of k will be loaded. The initialization circuit in Fig. 2 is for the clear-and-load function.

For the frequency synthesizer equipped with the modulo-N arithmetic, the maximal frequency is generated if $k = 2^R$, and the minimal frequency is obtained if $k = 1$. Thus, the ideal range of synthesized frequencies is

$$\frac{f_{mux\_out}}{2^{R+1}} \le f_z \le \frac{f_{mux\_out}}{2} \quad (2)$$

where a suitable choice of R will generate output frequencies with a range wider than that of the flying-adder-based frequency synthesizer with the same Δ [3].

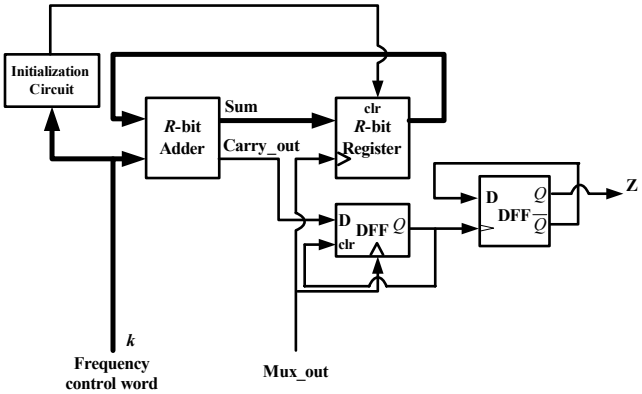

Figure 2: The modulo-N accumulator with the output stage of DFF.

The duty-cycle of the output frequency can also be controlled by a modified modulo-N accumulator with two frequency control words (k_1, k_2). The modulo-N accumulator with two frequency words for the duty-cycle control is depicted in Fig. 3. To select the frequency control word to achieve the desired duty-cycle, a multiplexer is added in Fig. 3, where the output signal **Z** controls the selection of the frequency control word to adjust the timing that **Z** stays at the high level.

In addition, the proposed architecture can also be modified to adapt itself to the case of a non-integer frequency control word, where another accumulator will be added to perform the summation of the fractional part of the frequency control word, and after a few cycles, the accumulation of the fractional part will result in a carrier that aligns the phase offset.

3. Analysis

Due to the possibility of non-zero remainders in the modulo-N arithmetic, the phase of the synthesized output may not align with the desired phase [1, p. 266], which leads to the inherent phase jitter.

Let $N = 2^R$. According to the modulo-N arithmetic, if d the great common divisor of N and k, then after N/d clocks, the remainder stored in the modulo-N accumulator is zero.

Let n denote the number of overflow pulses within the first time that the remainder reaches zero, and m_i denote the number of clocks that have passed when the i-th pulse appears

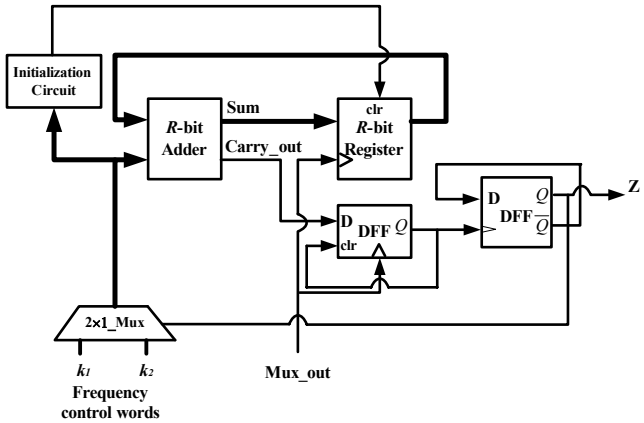

Figure 3: The modulo-N accumulator with the output stage of DFF.

for $i = 1, 2, \cdots n$. Then, n is the minimal integer which satisfies the equation

$$km_n = nN \quad \text{or} \quad \frac{m_n}{n} = \frac{N}{k} \quad (3)$$

where n is the value that makes nN the least common multiple (lcm) of k and N, i.e. $n = \text{lcm}(k, N)/N$. Consequently,

$$\sum_{i=1}^{n} m_i = \frac{\text{lcm}(k, N)}{k} \tag{4}$$

and the synthesized waveform will align with the desired phase after *n* overflow pulses.

If the desired frequency equals f_o, then the frequency control word can be obtained from the relation

$$\frac{k}{N} = \frac{2f_o}{f_{mux\_out}}. \tag{5}$$

For the *j*-th pulse, the phase offset is given by

$$\delta_j = \frac{m_j}{f_{mux\_out}} - \frac{j}{2f_o} \geq 0 \tag{6}$$

and $\delta_j = 0$ when $J = n$. This offset causes the inherent phase jitter. Let the average inherent phase jitter be defined by

$$\overline{\delta} = \frac{1}{n}\sum_{j=1}^{n} \delta_j \tag{7}$$

Denoted by r_i the remainder in the register of the modulo-*N* accumulator after the *i*-th pulse. Then, with (5), $\overline{\delta}$ can be written as

$$\begin{aligned} \overline{\delta} &= \frac{N}{\text{lcm}(k, N)} \sum_{j=1}^{\text{lcm}(k,N)/N} \left(\frac{m_j}{f_{mux\_out}} - \frac{j}{2f_o} \right) \\ &= \frac{1}{2f_o \cdot \text{lcm}(k, N)} \sum_{j=1}^{\text{lcm}(k,N)/N} r_j \end{aligned} \tag{8}$$

where the maximum $\overline{\delta}$ occurs as $k = N - 1$, i.e. $\overline{\delta}$ is bounded by

$$\overline{\delta} \leq \frac{1 + 2 + \cdots + (N-2)}{2f_o N(N-1)} = \frac{N-2}{4f_o N}. \tag{9}$$

Using the relation given by (5), we also obtain the maximum phase jitter as a function of the frequency control word as

$$\overline{\delta} \leq \frac{N-2}{2kf_{mux\_out}}. \tag{10}$$

From (9), $\overline{\delta}$ is smaller for smaller *N*, and $\overline{\delta} = 0$ for the special case of *N*=2.

4. Simulation and Numerical Results

In the simulation, a set of 32 reference waveforms (i.e., $M = 32$) is used with 32-to-1 multiplexer to generate f_{mux_out}, and $R = 4$ is employed for the modulo-*N* accumulator. The results of timing simulation with the TSMC 0.35μm cell-base process are presented for $k = 2, 4, 6, 8, 10, 12, 16$ in Fig. 4 to Fig. 9, respectively, where the frequency of reference waveforms is 151.5151 MHz. The maximal frequency obtained with k =16 is 75.697 MHz in Fig. 9. The inherent phase jitter can be observed in Fig. 7 and Fig. 8 for the cases of $k = 10$ and $k = 12$.

In Table 1, the corresponding values of the theoretical output period and the observed output period are summarized for different values of *k*. It is noticed that the observed periods are very close to the theoretical ones, which implies that the critical path and the delay from the logic operation are not serious.

Then, in Fig. 10, the maximum phase jitter given by (9) with $N = 16$ for different desired frequency is plotted. For larger desired frequency (e.g. $f_o > 50$MHz), the phase jitter can be lower than 5×10^{-3}.

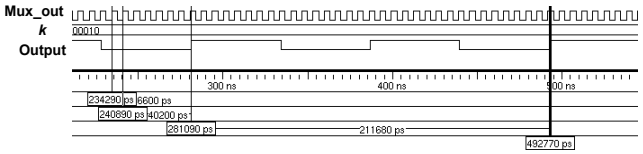

Figure 4: Results of timing simulations for *k* = 2.

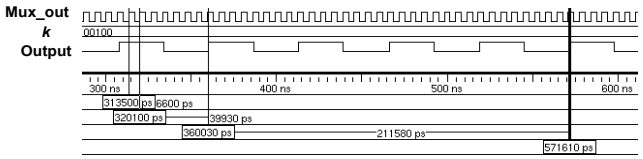

Figure 5: Results of timing simulations for *k* = 4.

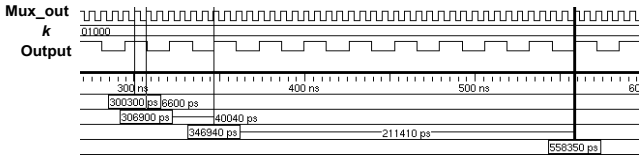

Figure 6: Results of timing simulations for *k* = 8.

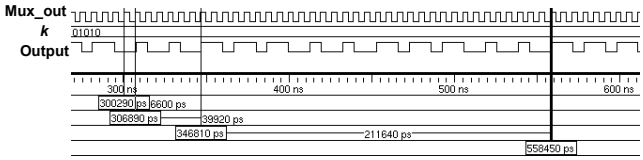

Figure 7: Results of timing simulations for *k* = 10.

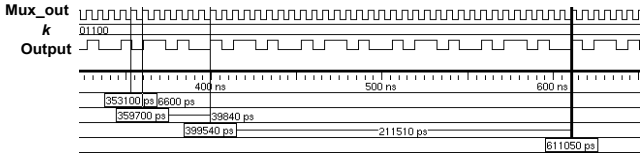

Figure 8: Results of timing simulations for *k* = 12.

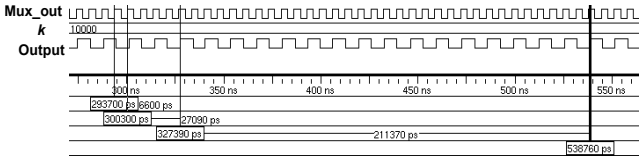

Figure 9: Results of timing simulations for *k* = 16.

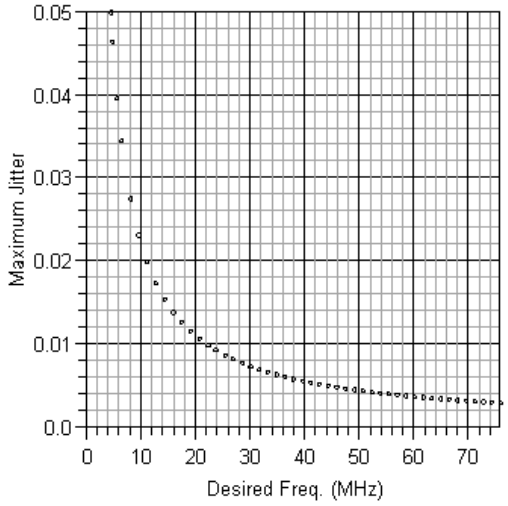

Figure 10 : The maximum inherent phase jitter for different desired frequency with N =16.

5. Conclusion

In this paper, by combining modulo-N arithmetic and the maximal frequency that can be generated by the flying-adder structure, a new architecture of the digital frequency synthesizer is devised. The new architecture will eliminate the glitch problem of the existing flying-adder structure while keep the chip area small and the power-consuming low. The proposed all-digital frequency synthesizer can also be applied to the realization of the direct digital frequency synthesizer, which is under investigation.

References

[1] V.F. Kroupa, *Phase Lock Loops and Frequency Synthesis* (Wiley, 2003).

[2] V.F. Kroupa, ed., *Direct Digital Frequency Synthesizers* (New York: IEEE Press, 1999).

[3] H. Mair & L. Xiu, An architecture of high performance frequency and phase synthesis, *IEEE J. Solid-State Circuits*, 35, 2000, 835–846.

[4] L. Xiu & Z. You, An flying-adder architecture of frequency and phase synthesis with scalability, *IEEE Trans. VLSI Syst.*,10, 2002, 637–649.

[5] L. Xiu & Z. You, A flying-adder frequency synthesis architecture of reducing VCO stages, *IEEE Trans. VLSI Syst.,* 13(2), 2005.

[6] Y.A. Chau, Ying-Yuan Yang, & Jeng-Fan Chen, All-Digital Frequency Synthesizer with Dual Resolutions, *Proc. of the IEEE ISPACS 2006,* Tottori Japan, 2006, 630-633.